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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/783,314	02/20/2004	Michael Warner	TESSERA 3.0-306 II CIP I	7827
38091	7590	11/17/2006	EXAMINER	
TESSERA LERNER DAVID et al. 600 SOUTH AVENUE WEST WESTFIELD, NJ 07090			SANDVIK, BENJAMIN P	
			ART UNIT	PAPER NUMBER
			2826	

DATE MAILED: 11/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/783,314

Applicant(s)

WARNER ET AL.

Examiner

Ben P. Sandvik

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 08 November 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 2-4, 8-12, 14-20 and 22 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 2-4, 8-11, 14-19 and 22 is/are rejected.
- 7) ☒ Claim(s) 12 and 20 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- ☒ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☐ Information Disclosure Statement(s) (PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- ☐ Notice of Informal Patent Application
- ☐ Other: \_\_\_\_\_

## DETAILED ACTION

### *Response to Arguments*

Applicant's arguments, filed 8/16/2006, with respect to the rejection(s) of claim(s) 1 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Hofstee.

### ***Claim Rejections - 35 USC § 102***

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 2, 9, and 17-19 are rejected under 35 U.S.C. 102(e) as being anticipated by Hofstee et al (U.S. PG Pub #2002/0074668).

With respect to **claim 2**, Hofstee teaches first semiconductor chip (Fig. 2, 204) having a front face, a rear face, edges bounding said faces and contacts exposed at said front face (Fig. 2, 208); a second chip (Fig. 2, 206), said second chip having front and rear surfaces and contacts (Fig. 2, 210) on said front surface, at least some of the contacts on said second chip being electrically connected to at least some of said contacts on said first chip, said front surface of said second chip facing upwardly and confronting a face of said first chip; a chip carrier (Fig. 2, plurality of signal posts 222) disposed below said rear surface of said second chip, said chip carrier having a bottom surface facing downwardly

away from said second chip and having a plurality of terminals exposed at said bottom surface for connection to a circuit panel (for connection to 224), at least some of said terminals being electrically connected to at least one of said chips (via connections 208), said chip carrier having an opening coinciding with at least a portion of said rear surface of said second chip; a circuit panel (Fig. 2, bottom substrate comprising 214, 224, 226, etc.) mounted to said bottom surface of said chip carrier, said circuit panel having a top surface and including a thermally conductive element (Fig. 2, 224) having a mounting surface extending in directions parallel to said top surface; and a flowable thermally conductive material uniformly covering at least a substantial portion of said rear surface (Fig. 2, plastic package 202), said flowable thermally conductive material connecting said rear surface of said second chip to said mounting surface of said thermally conductive element and spacing said rear surface of said second chip from said mounting surface, such that said rear surface of said second chip thermally communicates with said circuit panel through said flowable thermally conductive material.

With respect to **claim 9**, Hofstee teaches a configuration wherein a plurality of bottom chips (Fig. 2, 206) are provided under a top chip (Fig. 2, 204).

With respect to **claim 17**, Hofstee teaches that said front face of said first chip faces downwardly towards said front surface of said second chip.

With respect to **claim 18**, Hofstee teaches that said contacts of said first chip are bonded to said contacts of said second chip, said first chip being in

thermal communication with said second chip through said bonded contacts (Fig. 2, 208).

With respect to **claim 19**, Hofstee teaches a thermally conductive underfill between said first and second chips, said first chip being in thermal communication with said second chip through said underfill (Fig. 2, plastic housing 202).

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hofstee, in view of Ho et al (U.S. Patent #6657296).

With respect to **claims 3 and 4**, Hofstee does not teach a thermally conductive material including solder or a thermally conductive paste. Ho teaches a thermally conductive material that includes solder (Fig. 1, 24 and Col 3 Ln 11-13). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a material that includes solder as taught by Ho in order to enhance the thermal performance of the package.

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hofstee, in view of Ku et al (U.S. Patent #2003/0148578)).

With respect to **claim 8**, Hofstee does not teach that said second chip includes a plurality of passive electrical components. Ku teaches a microprocessor chip that includes passive components (Paragraph 27). It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide capacitors on the microprocessor chip of Hofstee as taught by Ku in order to decouple the signal in the chip.

Claims 10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hofstee, in view of Li (U.S. PG Pub #20020195700).

With respect to **claim 10**, Hofstee does not teach one or more discrete passive electrical components electrically connected to the terminals of said chip carrier. Li teaches a package with discrete passive electrical components connected to a chip carrier (Fig. 5, 506). It would have been obvious to one of ordinary skill in the art at the time the invention was made to connect passive components to the terminals of Hofstee as taught by Li in order to suppress unwanted radiation.

With respect to **claim 11**, Hofstee not teach one or more discrete passive electrical components electrically connected to at least one of said chips. Li teaches a package with discrete passive electrical components electrically connected to a chip (Fig. 5, 504). It would have been obvious to one of ordinary

skill in the art at the time the invention was made to connect passive components at least one of the chips of Hofstee as taught by Li in order to suppress unwanted radiation.

Claims 14-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hofstee, in view of Fukui et al (U.S. Patent #6100594).

With respect to **claim 14**, Hofstee does not teach that said rear face of said first chip faces downwardly towards said front surface of said second chip. Fukui teaches a stacked configuration wherein the first chip has a rear surface which faces the front surface of a second chip (Fig. 8b); comprising leads connecting at least some of said contacts of said first chip and at least some of said contact of said second chip (Fig. 8b, 18); further comprising a thermally-conductive layer between said rear face of said first chip and said front face of said second chip (Fig. 5, 6). It would have been obvious to one of ordinary skill in the art at time the invention was made to provide the chip of Hofstee in this configuration in order to reduce the length of bond wires and to adhere the chip together.

Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hofstee, in view of Kuan et al (U.S. PG Pub #20030047797).

With respect to **claim 22**, Hofstee does not teach that said first chip is a radio frequency amplifier chip. Kuan teaches a chip that is used as radio

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frequency amplifier chip (Paragraph 24). It would have been obvious to one of ordinary skill in the art at the time the invention was made to make the first chip of Hofstee a radio frequency amplifier chip as taught by Kuan in order to use the package to process a signal.

### ***Allowable Subject Matter***

Claims 12 and 20 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

### ***Conclusion***

**THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.



Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ben P. Sandvik whose telephone number is (571) 272-8446. The examiner can normally be reached on Mon-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272-1915. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

bps

  
**EVAN PERT**  
**PRIMARY EXAMINER**